1 CH Multi-Standard Analog HD Video Receiver with MIPI Interface

BM7111

Application Note

Rev 0.3

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Contents

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1. Output Mode of BM7111

The BM7111 provides two kinds of output mode such as parallel mode and MIPI mode. The parallel output mode and MIPI output mode shares the same output pins (VD[7:0], VDCK0/1) so that both output modes cannot be supported simultaneously.

1.1. Parallel Output Mode

For parallel mode, one channel output and two channel multiplexed output can be supported. In one channel output mode, the data format can be ITU-R BT.656 or ITU-R BT.1120 standard. In two channel multiplexed mode, the data format can also be ITU-R BT.656 or ITU-R BT.1120 with channel ID in the SAV/EAV code as shown in the Table 1 and Table 2. In multiplexed mode, the different resolution video data (SD, HD720p and HD1080p) can be multiplexed through conversion from lower resolution (SD or HD720p) video data rate (8bit@27MHz or 74.25MHz) to higher resolution (HD1080p) video data rate (8bit@148.5MHz). In other words, all video data of multi-channel are synchronous so that they can be multiplexed and only one clock is used for it. In multiplexed mode, the video output data is triggered at rising or falling edge of clock for SDR (Single Data Rate) mode, but it is triggered at both rising and falling edge for DDR (Dual Data Rate) mode. The two channel multiplexed mode is available only for multi-chip cascaded application. The Fig 1 and Fig 2 show the timing diagram of two channel multiplexed format for SDR and DDR mode.

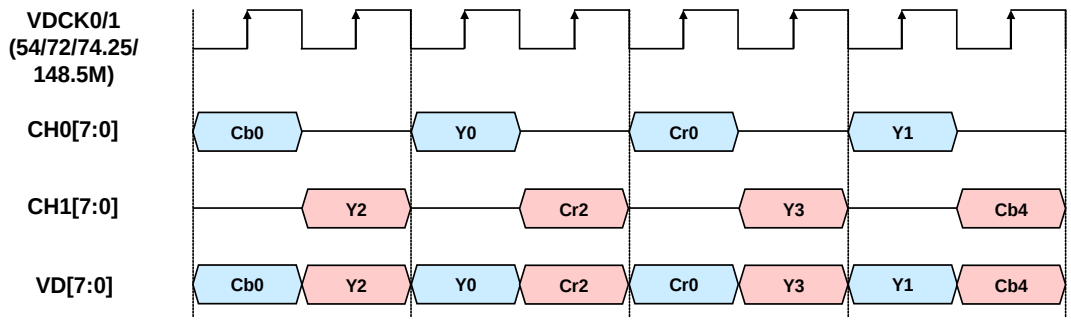

Fig 1. Timing Diagram of Two Channel Multiplexed Format for SDR Mode

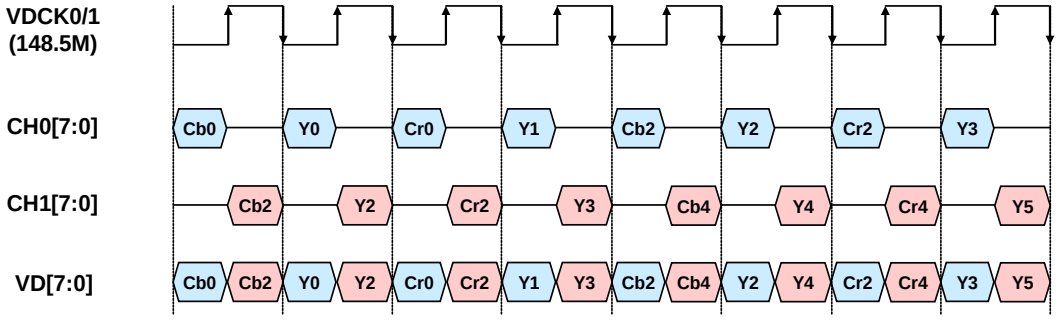

Fig 2. Timing Diagram of Two Channel Multiplexed Format for DDR Mode

Table 1. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.656 Format

Condition			FVH Value			SAV/EAV Code Sequence for Four CH Format				
Field	V time	H time	F	V	H	1st	2nd	3rd	4th	
									CH1	CH2
Even	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h
		SAV			0				E0h	E1h
	Active	EAV		0	1				D0h	D1h
		SAV			0				C0h	C1h
Odd	Blank	EAV	0	1	1				B0h	B1h
		SAV			0				A0h	A1h
	Active	EAV		0	1				90h	91h
		SAV			0				80h	81h

Table 2. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.1120 Format

Condition		VH Value		SAV/EAV Code Sequence for Four CH Format				
V time	H time	V	H	1st 2nd	3rd 4th	5th 6th	7th/8th	
							CH1	CH2
Blank	EAV	1	1	FFh	00h	00h	B0h	B1h
	SAV		0				A0h	A1h
Active	EAV	0	1				90h	91h
	SAV		0				80h	81h

1.2. MIPI Output Mode

The BM7111 supports a MIPI interface compliant with MIPI CSI2 V1.00 standard and DPHY V1.00.00 standard with 1 clock lane and 4 data lane. The max data rate of MIPI data lane is up to 297Mbps in HS transmission with YUV 422-8bit format. The **four data lane** should be used for **1920x1080@25/30Hz** format and **two data lane** can be used only for **1280x720@25/30Hz** or **SD** format. The multi-chip cascaded connection is not available in MIPI interface because the MIPI interface does not support the multiplexed output. The Fig 3 shows the detailed data payload structure of YUV422 8bit frame format in the long packet.

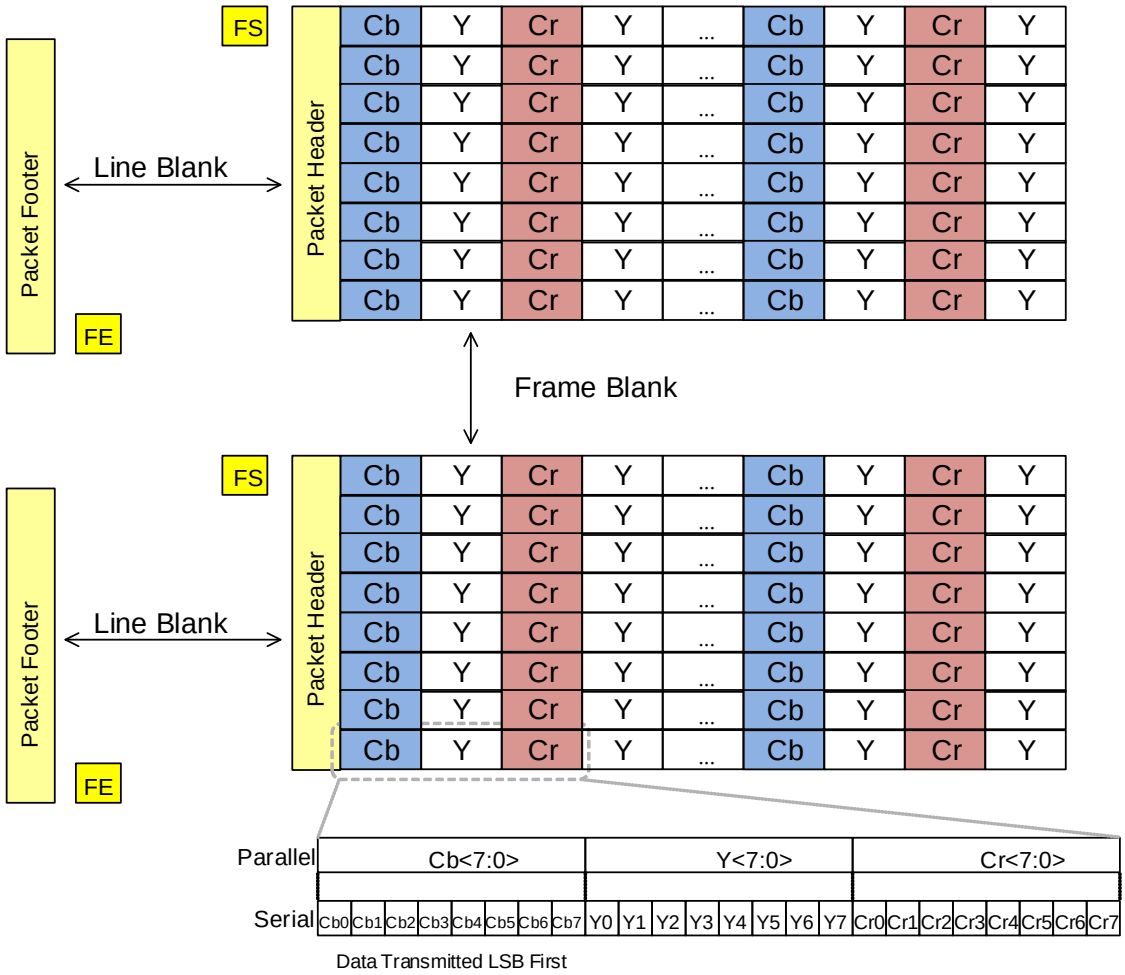

Fig 3. YUV422 8 Bit Frame Format for MIPI Transfer

The Fig 4 and Fig 5 describe the MIPI data lane transmission order for 4 lane and 2 lane mode.

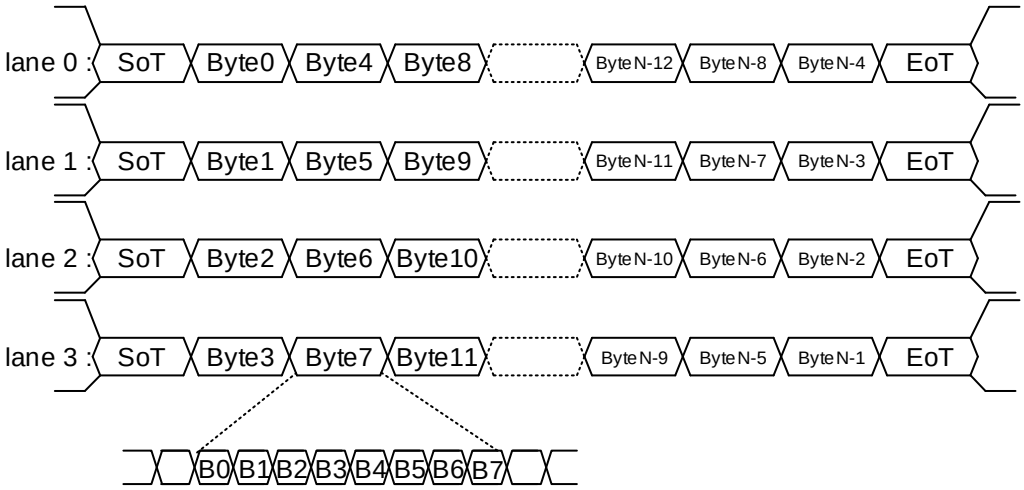

Fig 4. MIPI Data Lane Transmission Order for 4 Lane Mode

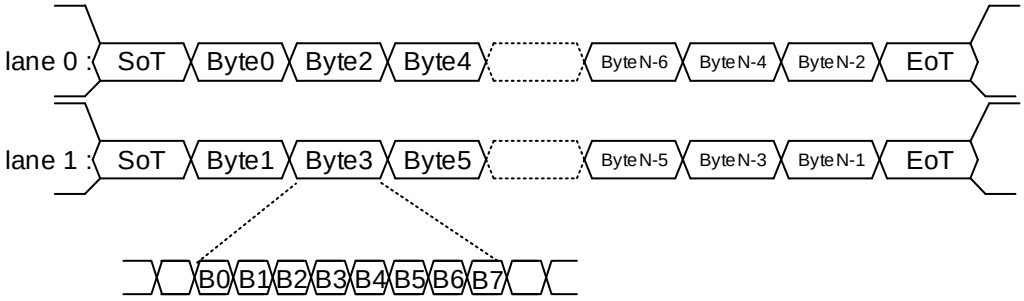

Fig 5. MIPI Data Lane Transmission Order for 2 Lane Mode

2. Multi-chip Cascaded Connection

The BM7111 provides a multi -chip cascaded operation supporting channel multiplexed output mode to reduce the interface pin count with back-end chipset only in case of parallel output mode. The multi-chip cascaded connection is not supported in MIPI output mode. The concept of multi-chip cascaded connection is illustrated in Fig 6.

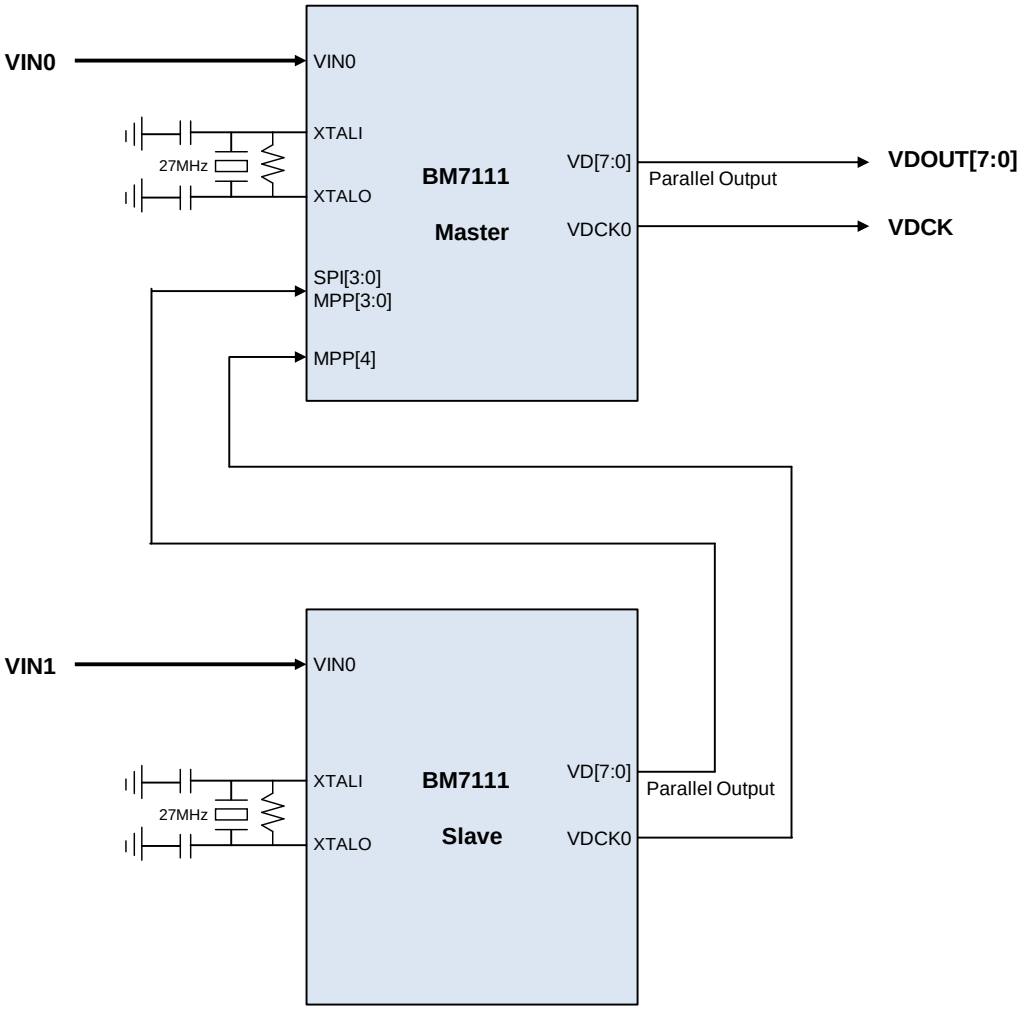

Fig 6. Cascade Connection for Multi-chip Application

The master and slave device can use each independent crystal oscillator thanks to asynchronous processing of data and clock in master device. The master device also supports the single data output with channel switching between master and slave output instead of channel multiplexing.

3. Application for 1.8V IO Supply Voltage

The BM7111 has four IO power domain s as shown in Fig 7. The VDDO1 (#16) in power domain1 should use only 3.3V IO voltage because the XTALI/O pad requires the 3.3V supply voltage. The VDDO2 (#28) in power domain2 can use 3.3V or 1.8V IO voltage for parallel output mode, but should use only 3.3V IO voltage for MIPI output mode. The VDDO3 (#36) in power domain3 can use either 3.3V or 1.8V IO voltage. For 1.8V IO supply voltage mode in power domain2 or 3, the data interface pin has 0 ~ 1.8V voltage range (0V for logic Low and 1.8V for logic High). The VDD1V (#3) and VDD1P (#8) in power domain4 should be applied with 1.2V and VDD3V (#5) and VDD3P (#9) in power domain4 should be applied with 3.3V for proper analog IP (Video ADC and PLL) operation. The reference schematics for 1.8V IO supply voltage are illustrated in Fig 8 and Fig 9. The multi-chip cascaded connection is not supported with 1.8V IO supply voltage.

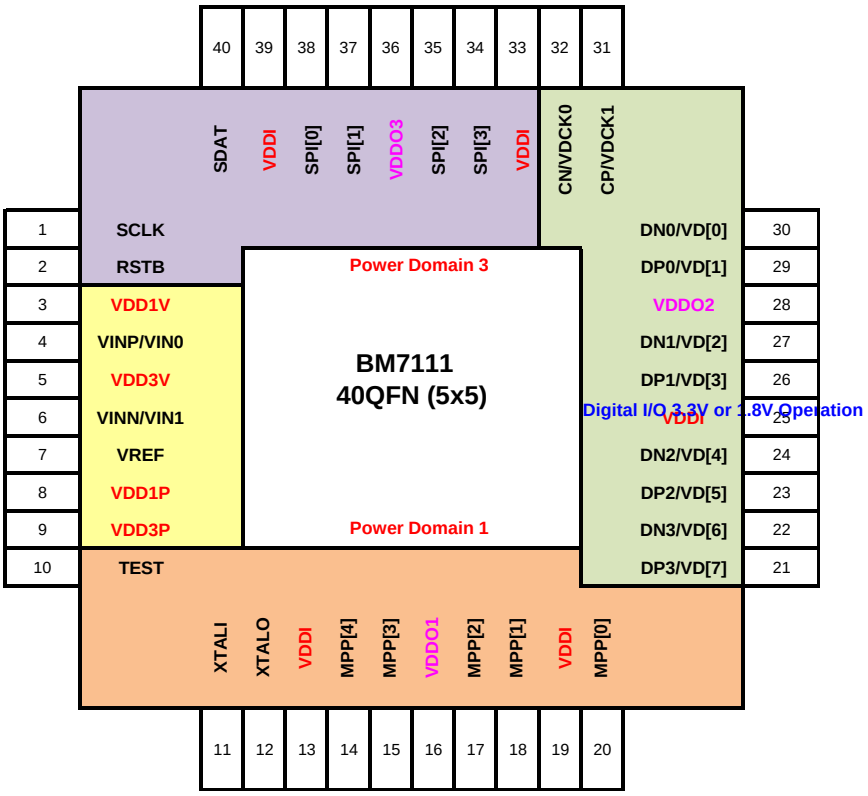

Fig 7. Power Domain of BM7111

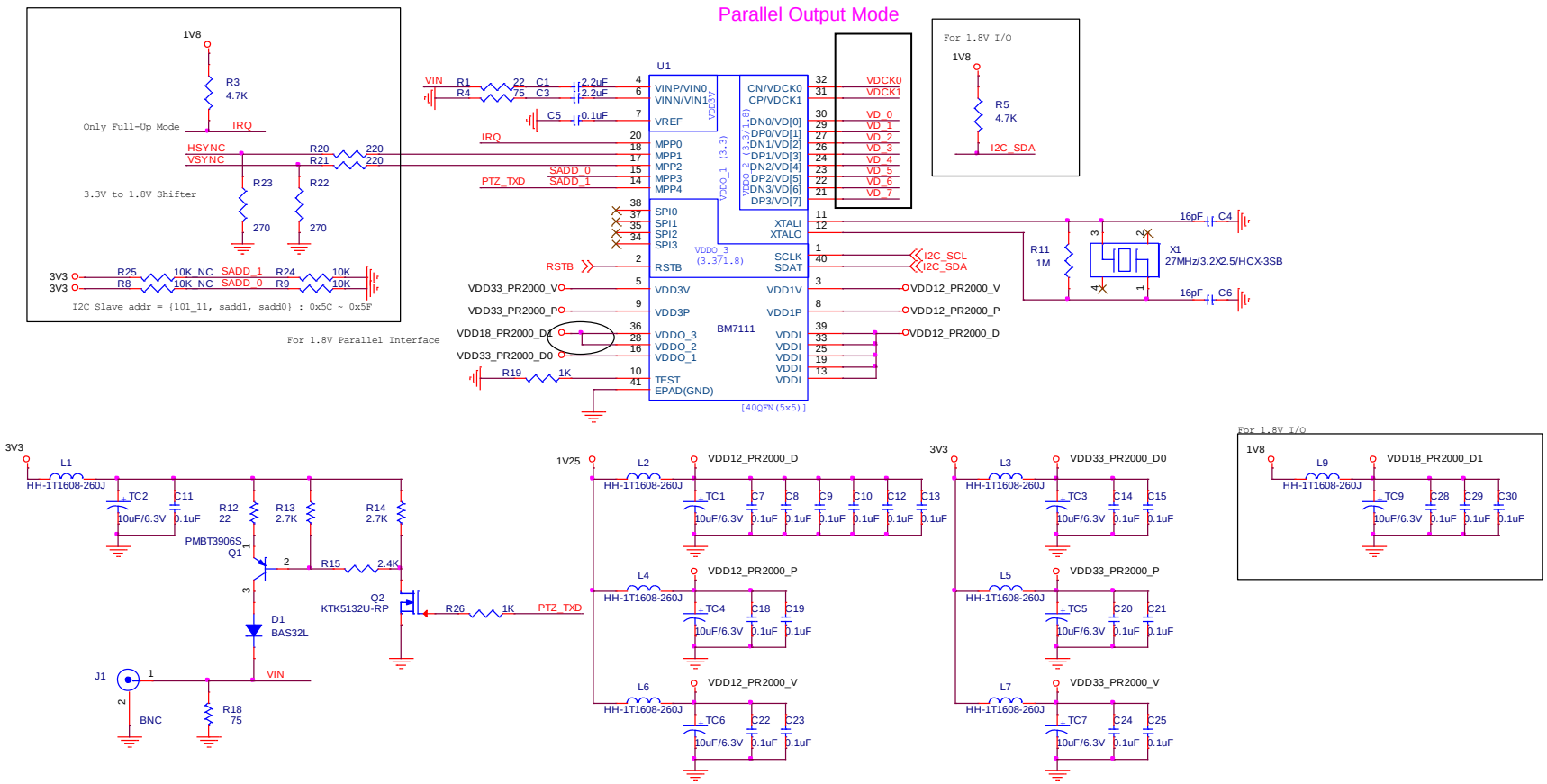

Fig 8. Reference Schematic of 1.8V IO Supply Application for Parallel Output Mode

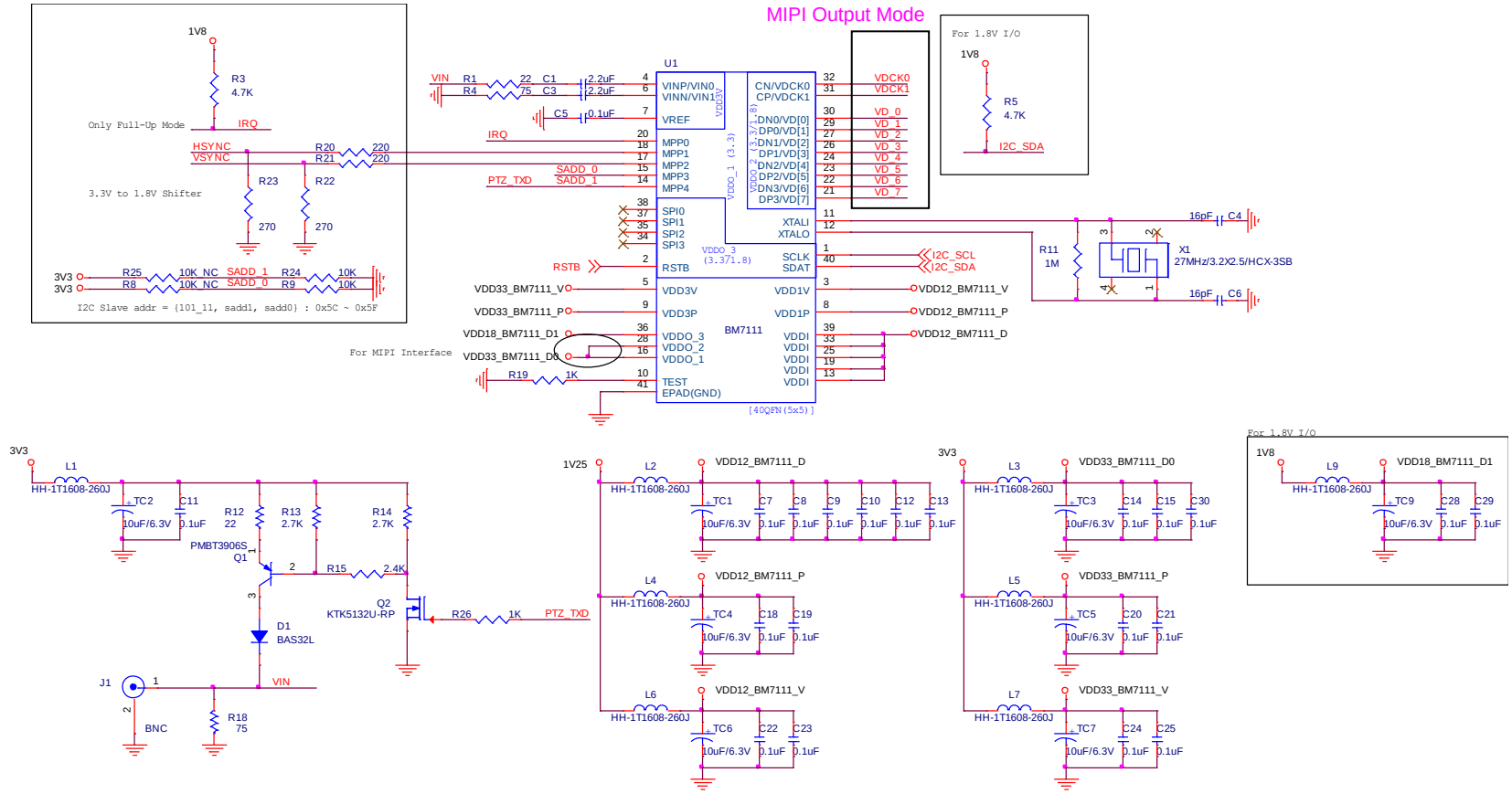

Fig 9. Reference Schematic of 1.8V IO Supply Application for MIPI Output Mode

4. Revision History

Version	Date	Description
V0.1	2017.02.24	First Edition is Released
V0.2	2017.03.07	Application for 1.8V IO Supply Voltage is Added (P.9 ~ 11)
V0.3	2017.04.20	Voltage for VDD1V, VDD1P, VDDI Voltage is Change from 1.2V to 1.25V (P.10 ~ 11)